

FIG.1

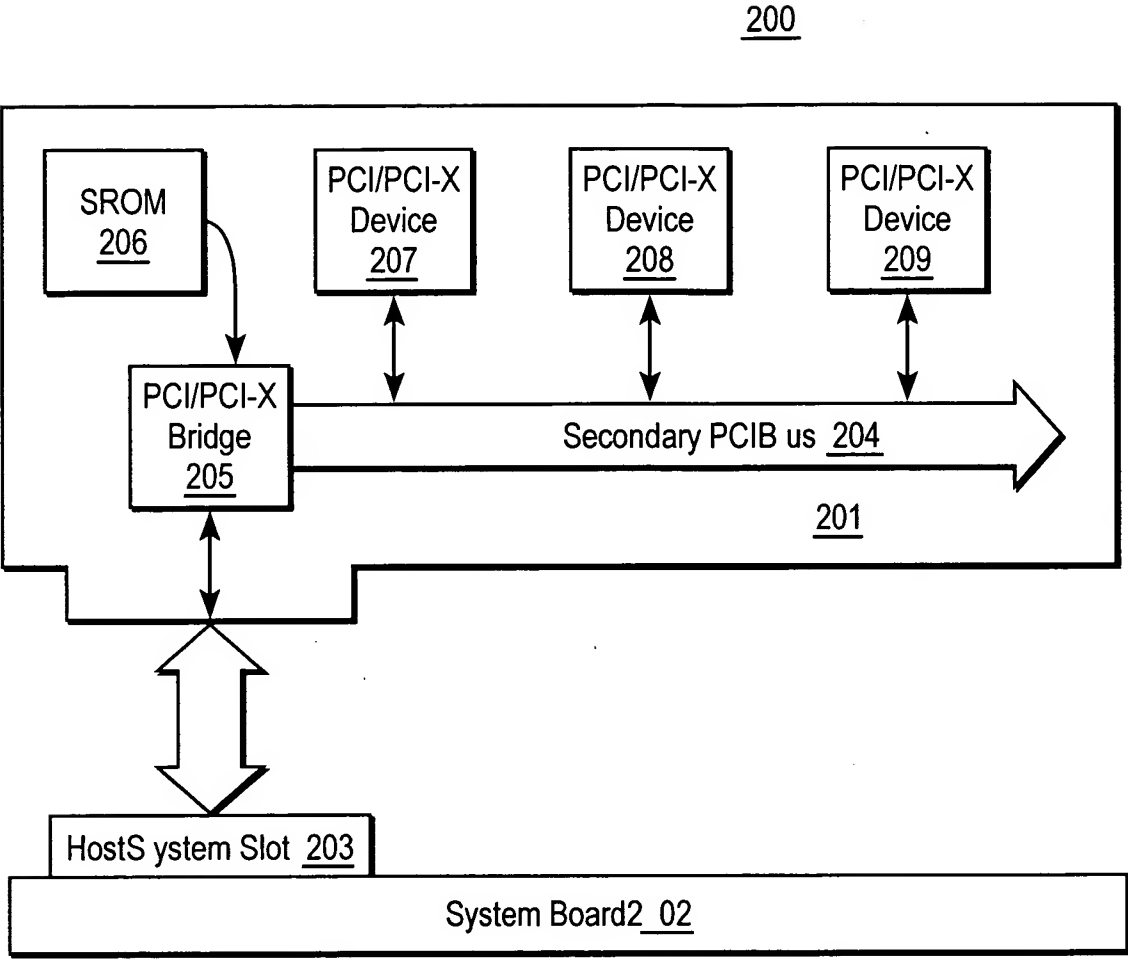


FIG.2

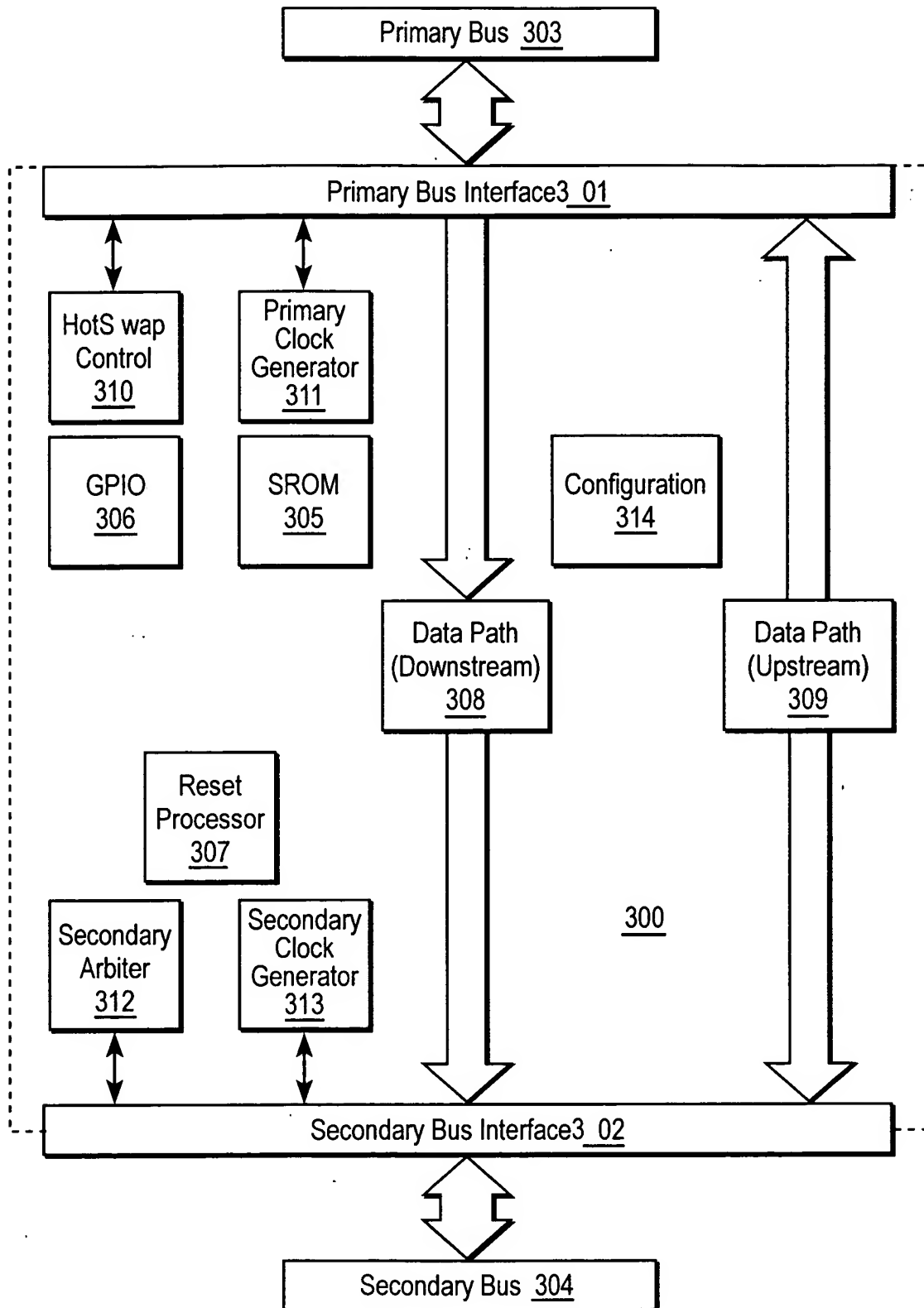


FIG. 3

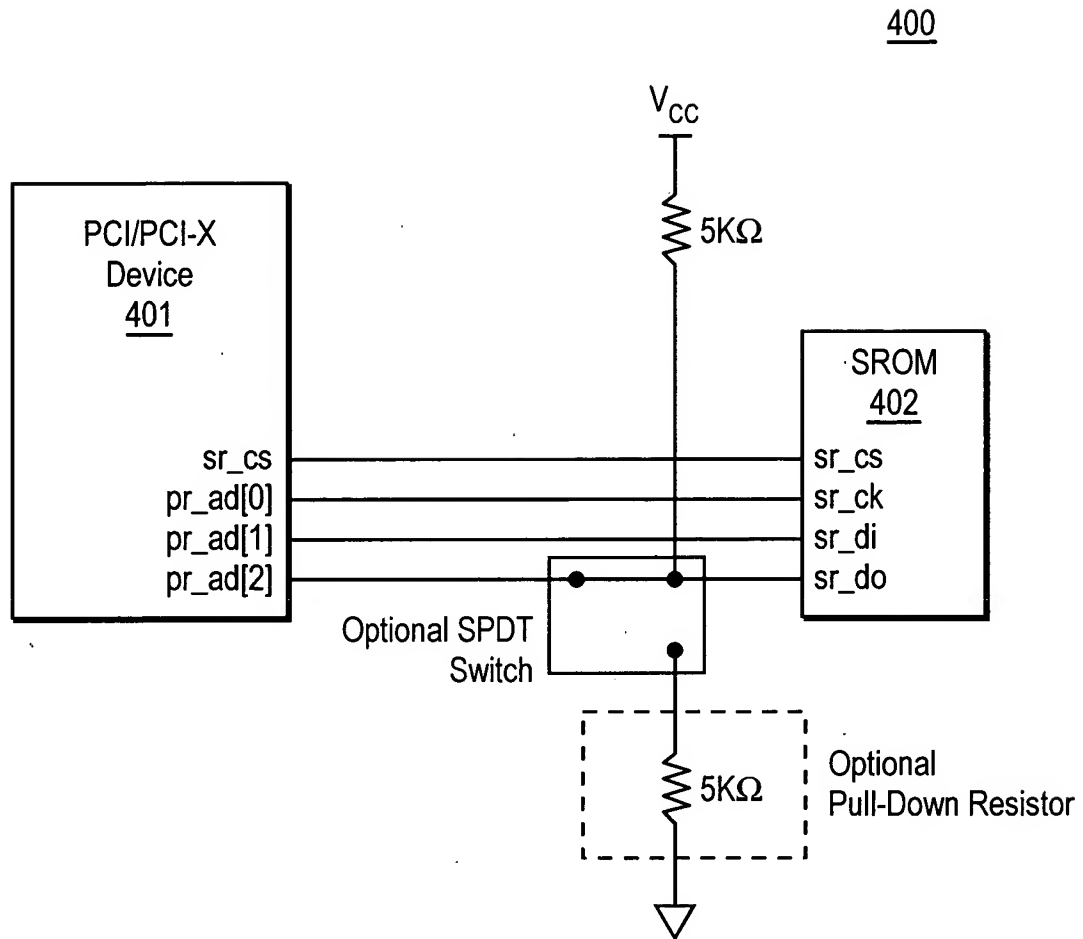


FIG.4

Byte offset	Description
00h	[7:6] 1 0b to enable serial pre-load [5:0] 0 00001b (load Vendor ID/Device ID/Device ID/Revision ID) [5:0] 0 00000b (Reserved) <span style="float: right;">501</span>
01h	Arbiter Control / Status[7:0]
02h	Arbiter Control / Status[15:8]
03h	31154 Control Register 0
04h	31154 Control Register 1[7:0]
05h	31154 Control Register 1[15:8]
06h	31154 Control Register 2[7:0]
07h	31154 Control Register 2[15:8]
08h	Multi-Transaction Timer Register[7:0]
09h	Multi-Transaction Timer Register[15:8]
0Ah	Pre-Fetch Policy Register[7:0]
0Bh	Pre-Fetch Policy Register[15:8]
0Ch	P_SERR# Assertion Control Register[7:0]
0Dh	P_SERR# Assertion Control Register[15:8]
0Eh	Secondary IDSEL Select Register[7:0]
0Fh	Secondary IDSEL Select Register[15:8]
10h	Secondary IDSEL Fnct0 Enable Register[7:0]
11h	Secondary IDSEL Fnct0 Enable Register[15:8]
12h	GPIO Pin Configuration Register
13h	GPIO Write One to Toggle Register
14h	Opaque Memory Base and Limit Register[7:0]
15h	Opaque Memory Base and Limit Register[15:8]
16h	Opaque Memory Base and Limit Register[23:16]
17h	Opaque Memory Base and Limit Register[31:24]
18h	Opaque Memory Base Upper 32 Bits[7:0]
19h	Opaque Memory Base Upper 32 Bits[15:8]
1Ah	Opaque Memory Base Upper 32 Bits[23:16]
1Bh	Opaque Memory Base Upper 32 Bits[31:24]
1Ch	Opaque Memory Limit Upper 32 Bits[7:0]
1Dh	Opaque Memory Limit Upper 32 Bits[15:8]
1Eh	Opaque Memory Limit Upper 32 Bits[23:16]
1Fh	Opaque Memory Limit Upper 32 Bits[31:24]
20h	Slot Number Register
21h	Chassis Number Register
22h	Power Management Next Item Pointer. Must be pre-loaded with a value of 4h to expose VPD register block to software.
23h	Power management Capabilities Register[15:8] This register may be pre-loaded with high order bits [15:11] set to 1111b indicating that the bridge supports PME# generation from any PM DState. This feature may be used to workaround a Windows 98 bridge power management errata.
24h	ID [7:0] The Device ID and Vendor ID are only preloaded if SROM offset 0 0h = 1000_0001. Otherwise, offsets 24h-28h are ignored.
25h	ID [15:8]
26h	ID [23:16]
27h	ID [31:24]
28	RID The Revision ID is only preloaded if SROM offset 0 0h = 1000_0001. Otherwise, offsets 24h-28h are ignored.
29h - 7Fh	Reserved.
80h - 0FFh	Vital Product Data (Read Only region).
100h - 1FFh	Vital Product Data (Read/Write region).

500

FIG.5

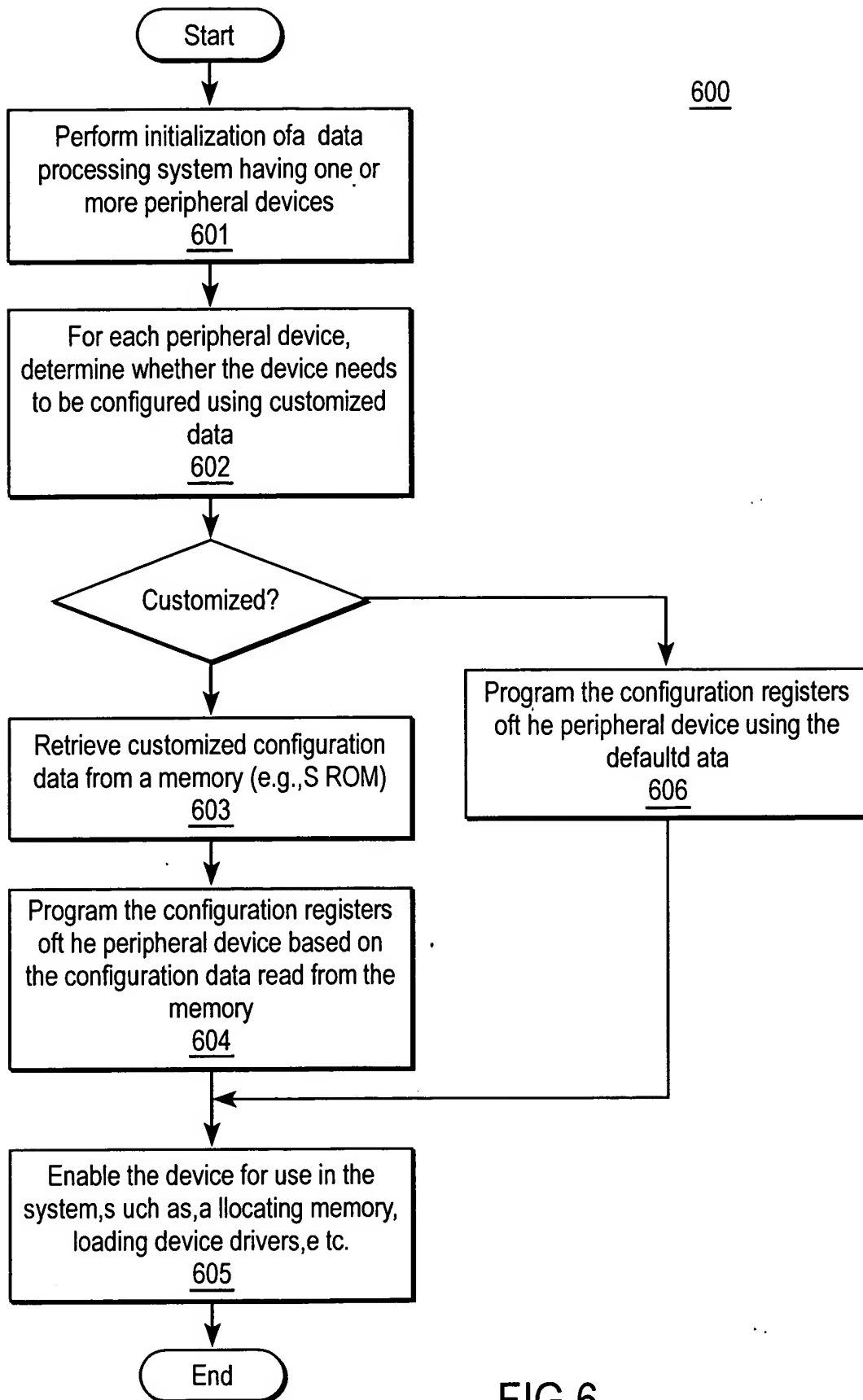


FIG.6